EFFECT OF SYSTEM DESIGN AND TEST CONDITIONS ON WAFER LEVEL PACKAGE DROP TEST RELIABILITY

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ABSTRACT
The effects of system design and drop test (DT) conditions on wafer level package (WLP) DT reliability are studied through DT experiments and finite element analysis (FEA). It is concluded that the failure rate of corner components on JEDEC board is inversely proportional to the corner component distance to the nearest mounting hole. BGA packages mounted in proximity to WLP affect WLP DT performance. A larger BGA mounted directly beneath the WLP significantly improves WLP DT life. However, when the BGA mount location partially overlaps with the WLP, WLP DT life is reduced. In this case the solder joint cracks at the WLP edge away from the BGA are significantly accelerated by the BGA. Face-up drop results in earlier failures for corner components than that in face-down drop. But for the central component group in the JEDEC board, it shows slight better performance.

Key words: WLP, drop test, reliability

INTRODUCTION
Wafer level packages (WLP) are increasingly accepted in portable electronics due to its small form factor and low manufacturing cost. Drop test (DT) performance has been the key package reliability indicator for portable applications. In order to fully assess the DT reliability, it is helpful to understand the factors that influence the DT readings. These factors are classified to three levels.

Level 1 – package factors
1. Package construction and material
2. Package size
3. Die size
4. Solder ball material composition
5. Underfill
6. Process parameters and history (Namely if the package has been stressed)

Level 2 – system design factors
1. 1.

distributions are not consistent among test groups. The number of drops to 5% failure at 90% confidence level incorporates the elements of both first failure and characteristic life, and thus, it is more suitable parameter for characterizing DT life. In this study, DT lives are normalized to simplify the comparison.

In the subsequent discussion, studies on the effect of system design and test conditions are presented. Effect of WLP placement is studied.

EFFECT OF SYSTEM DESIGN AND DROP CONDITIONS

Effect of WLP placement locations on PCB

PCB outline and component placement box defined by JEDEC[1] is shown in Figure 1. Based on the symmetry, the 15 components are classified in six groups (A-F in Figure 1). Distance between the corner components and the mounting hole of 5 mm in both x and y is specified. In this study the effect of the distance from corner component to mounting

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discussed first. FEA results are used to verify the observations from the experiments.

Figure 4. Side view and top view of BGA mounting locations for legs 2 ï 4.

6.4x6.4 mm body 16x16 array 0.4 mm pitch daisy chain WLP is considered as the test vehicle. They are assembled to the JEDEC DT boards. BGA packages are then attached to the DT boards to investigate the effect of secondary components in the proximity of WLP on WLP DT reliability. Four legs are considered. Leg 1 is the reference leg where no BGA is attached. Legs 2-4 have BGAs mounted at nine middle WLPs on opposite side of the PCB. The locations of the BGAs relative to the WLPs are illustrated in Figure 4. For leg 2, the BGA is placed directly beneath the WLP. For leg 3, half of the WLP overlaps with the BGA. For leg 4, only one quarter of the WLP overlaps with the BGA. Data for groups B, E, and F are used to calculate the DT life.

Figure 5 shows the WLP DT lives for legs 1 ï 4. It is seen that the DT life is improved by nine times when the BGA is mounted directly under the WLP. However, when the WLP has partial overlap with the BGA, the drop life is reduced by more than half. Between the two legs with WLP partially overlapping the BGA, leg 4 which has less overlap gives slightly better DT life.

Figure 5. WLP DT life for DOE legs with different mounting options for 16x16 mm BGA.

Solder joint crack maps (Figures 6 and 7) are presented next to further understand the effect of BGA mounting with offset from WLP (legs 3 and 4). For leg 3 where half of WLP body overlaps the BGA, there is more damage on solder joints next to WLP right edge which is away from the BGA. This may be because the BGA stiffens the PCB around BGA footprint. And the PCB bends less in this area during drop. More bending happened on PCB elsewhere especially at WLP right edge that is away from BGA. This results in larger peeling stress on solder joints along this edge, which in turn caused more solder joint cracks at WLP right edge. The crack map for leg 4 (Figure 7) shows that there are more solder joint cracks along right and bottom edges which are away from the BGA. This observation is

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inline with leg 3. The leg 4 has longer DT life which may be due to less PCB stiffening at WLP footprint, compared to leg 3.

It is interesting to see significant DT life improvement in leg 2 where a BGA much larger than the WLP is mounted directly underneath the WLP. At this point, it is important to understand the difference due to a BGA smaller than the WLP. 4x4 mm BGA are mounted to directly underneath the WLPs and DT was conducted. The comparison between 4x4 and 16x16 mm BGA is given by Figure 8. It is seen that when 4x4 mm BGA is mounted, the DT life for WLP has trivial improvement only. This is very different from leg 2 where larger BGAs are considered.

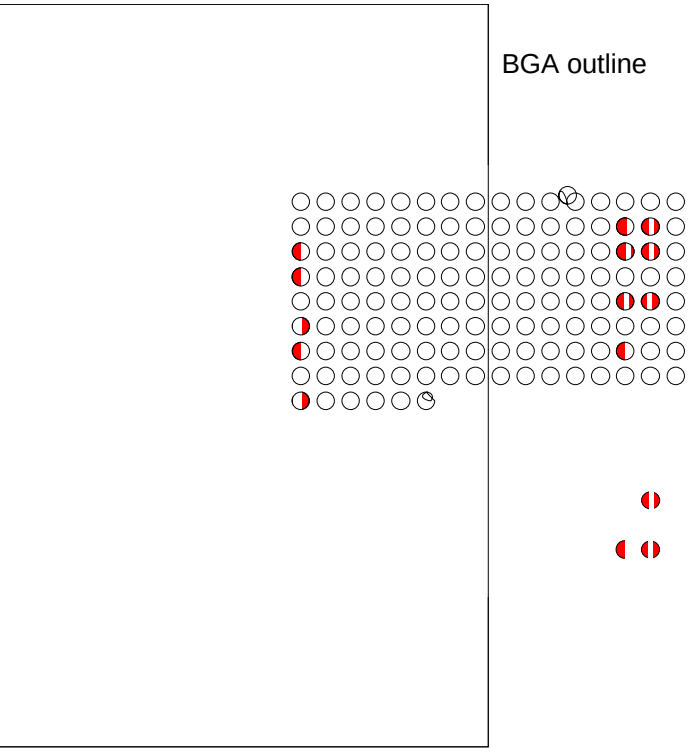

Figure 6. Solder joint crack map for U13 of leg 3.

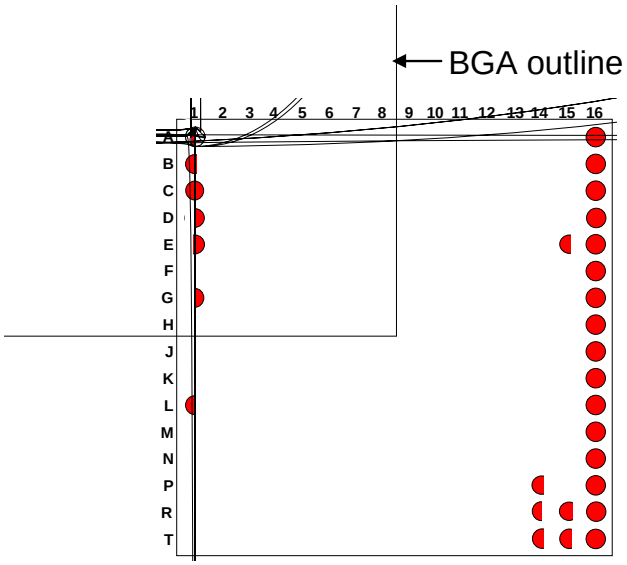

Figure 7. Solder joint crack map for U8 for leg 4.

In order to better understand, FEA is performed for cases with BGA mounted directly underneath the WLP. In this FEA work, WLP body size is 6x6 mm. Two BGA sizes are considered, 8x8 and 5x5 mm. The FEA results are plotted in Figure 9. It is interesting to see that when the BGA is smaller than the WLP, the peeling stress is reduced only slightly. The DT life in this case is expected stay approximately the same as reference case where there is no BGA. However, when the BGA is greater than the WLP, the peeling stress for WLP is significantly reduced. And the DT life in this case is expected to be much greater. The FEA results are inline with the experiment (Figure 8).

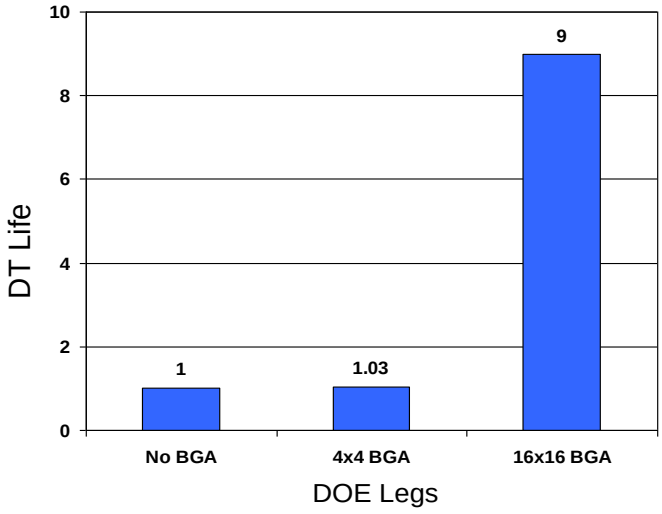

Figure 8. Comparison between BGA larger and smaller than WLP in size. BGA is centered on WLP.

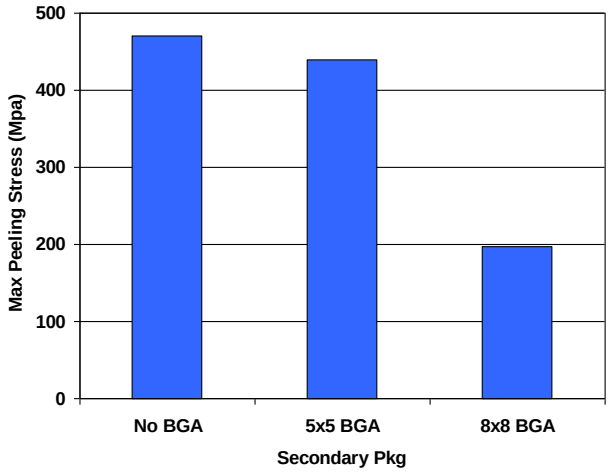

Figure 9. FEA results - solder joint maximum peeling stress calculated by FEA for cases with different size BGAs mounted directly under the WLP.

To better explain this trend, PCB bending is examined. Figure 10 shows the PCB in-plane normal strain in x horizontal direction $_x$. $_x$ is proportional to the degree of PCB bending which is responsible for DT damage. It is observed from Figure 10 that when the 5x5 mm BGA is present, there is trivial difference compared to no BGA (a) in $_x$ at WLP footprint indicating that the small BGA results in trivial PCB stiffening. On the other hand when the 8x8 mm BGA is present, the PCB $_x$ is significantly reduced due to added stiffness from the BGA. The $_x$ at WLP corner solder joint is much lower than that when no BGA present. The reason for the stress reduction may be that the stiffness of the PCB is increased by the BGA at WLP footprint and around the WLP. This results in less PCB bending at critical solder joint locations during drop, which in turn reduces the solder joint peeling stress. This results in improved DT life.

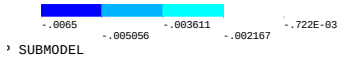

Figure 10. FEA results - strain $_x$ plot of PCB at the areas of WLP and BGA. (a) No BGA, (b) 5x5 mm BGA mounted under WLP, and (c) 8x8 mm BGA mounted under WLP.

Effect of Drop Orientation

JESD22-B111 standard specifies component face down during drop. It is of interest to understand the difference due to a different orientation. For this reason, DT is performed for component face up and down orientations. Again the 16x16 array 0.4 mm pitch WLP is considered as the test vehicle. The DT data for these two drop orientations are plotted in Figure 11.

It is seen from Figure 11 that the failure rate for center component (group F) is higher in face down than face up drop orientation. However, corner group A fails much earlier compared to face down orientation. Therefore, DT reliability varies with drop orientations. Optimizations done based on JEDEC standard drop orientation may not be valid for applications with different drop orientation.

Figure 11. DT comparison between components facing up and down for groups A and F WLP. 16x16 array 0.4 mm pitch WLP is considered as the test vehicle.

To explain the difference, it is useful to understand how PCB bending causes the solder joint failures during DT. PCB bending during drop is illustrated in Figure 12. WLP and solder joint shapes of corner and center components are included for options of component face down (dark color) and face up (light color) options. As is seen, the PCB is fixed to the drop table at four corners by mounting screws. After drop impact, the PCB vibrates. It first bends downward (first bend), and then upward (second bend). During the first bend, the PCB has positive curvature in the middle and negative curvature at corners. And it is opposite at the second bend. The vibration attenuates and the second bend has smaller magnitude.

In general, solder joint fracturing during DT is caused by peeling stress due to PCB bending. The corner solder joints

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4. Drop orientation makes difference in DT life. Component face up orientation is more critical for